DEBAPRIYA CHATTERJEE

PERSONAL PROFILE

Name: Debapriya Chatterjee Tel. No.:001-734-223-6451

Address: Apt #3307
12430 Metric Boulevard
Austin, TX 78758, USA

Primary E-Mail: chatterjee.debapriya@gmail.com
Alternate E-Mail: dchatt@umich.edu

EDUCATION

- Ph.D. in Computer Science and Engineering - University of Michigan – Area: Hardware – Dissertation title "Harnessing Simulation Acceleration to Solve the Digital Design Verification Challenge" - Advisor: Prof. Valeria Bertacco – graduated in May 2013
- M.S. (Master of Science) in Computer Science and Engineering – University of Michigan - Area: Hardware – GPA 3.7/4.0 (converted from 9.0 scale)– graduated in 2010
- B. Tech. (Bachelor of Technology) - Indian Institute of Technology (IIT), Kharagpur, India – Major: Computer Science and Engineering – GPA 9.07/10.0 - graduated in 2007

PUBLICATIONS

- **Boosting simulation based validation performance and engineering effort**

Improving validation/debug support beyond software simulation (acceleration/emulation /post-silicon validation, where performance is increasing but visibility is decreasing):

- **"ArChiVED: Architectural Checking via Event Digests for High Performance Validation"** in Design Automation and Test in Europe **(DATE) 2014** by Chang-Hong Hsu, **Debapriya Chatterjee**, Ronny Morad, Raviv Gal and Valeria Bertacco
- **"Hybrid Checking for Microarchitectural Validation of Microprocessor Designs on Acceleration Platforms"** in International Conference on Computer Aided Design **(ICCAD) 2013** by **Debapriya Chatterjee**, Biruk Mammo, Doowon Lee, Raviv Gal, Ronny Morad, Amir Nahir, Avi Ziv and Valeria Bertacco
- **"Checking Architectural Outputs Instruction-By-Instruction on Acceleration Platforms"** in Design Automation Conference **(DAC) 2012** by Debapriya Chatterjee, Anatoly Koyfman, Ronny Morad, Avi Ziv and Valeria Bertacco
- **"Approximating Checkers for Simulation Acceleration"** in Design Automation and Test in Europe **(DATE) 2012** by Biruk Mammo, **Debapriya Chatterjee**, Dmitry Pidan, Amir Nahir, Avi Ziv, Ronny Morad and Valeria Bertacco
- **"Simulation-based Signal Selection for State Restoration in Silicon Debug"** in International Conference on Computer Aided Design **(ICCAD) 2011** by **Debapriya Chatterjee**, Calvin McCarter and Valeria Bertacco

Towards achieving accelerated simulation:

- **"Gate-level Simulation with GPU computing"** in ACM Transactions on Design Automation of Electronic Systems**(TODAES)** volume 16 issue 3, June **2011** by **Debapriya Chatterjee**, Andrew DeOrio, Valeria Bertacco

- **"High Performance Gate-Level Simulation with GP-GPUs"** as a book chapter in **GPU Computing Gems** by **Debapriya Chatterjee**, Andrew DeOrio, Valeria Bertacco (publisher Morgan Kaufmann, 2010)
- **"Event-driven Gate-level Simulation with GP-GPUs"** in Design Automation Conference **(DAC) 2009** by **Debapriya Chatterjee**, Andrew DeOrio, Valeria Bertacco
- **"GCS: High-performance Gate-level Simulation with GP-GPUs"** in Design Automation and Test in Europe **(DATE) 2009** by **Debapriya Chatterjee**, Andrew DeOrio, Valeria Bertacco
- **"SAGA: SystemC Acceleration on GPU Architectures"** in Design Automation Conference **(DAC) 2012** by Sara Vinco, **Debapriya Chatterjee**, Valeria Bertacco and Franco Fummi
- **"SystemC Simulation on GP-GPUs: CUDA vs OpenCL"** to appear in **CODES+ISSS 2012** by Nicola Bombieri , Sara Vinco, Valeria Bertacco and **Debapriya Chatterjee**

Application of accelerated simulation to pre-silicon validation:

- **"EQUIPE: Parallel Equivalence Checking with GP-GPUs"** *in* IEEE International Conference on Computer Design **(ICCD) 2010** by **Debapriya Chatterjee** and Valeria Bertacco

❖ **Fast verification methodologies using semi-formal methods and simulation**:

- **"Activity-based Refinement for Abstraction-guided Simulation"** in IEEE High-level Design Verification and Test workshop **(HLDVT) 2009** by **Debapriya Chatterjee** and Valeria Bertacco

PATENTS

- US Patent `8738349 B2`, "Gate-level Logic Simulator using Multiple Processor Architectures" by Valeria Bertacco, Debapriya Chatterjee, Andrew Deorio
- US Patent `8601418 B1`, "Instruction-by-Instruction Checking on Acceleration Platforms" by Debapriya Chatterjee, Anatoly Koyfman, Ronny Morad, Avi Ziv

MAJOR PROJECTS

- [Jan 2012- Feb 2013] Worked on adapting traditional pre-silicon software-based verification environments such as complex UVM testbenches for large designs to an acceleration / emulation environment using a synergistic combination of in-place hardware checking, compact trace collection and post-simulation checkers.
- [July 2011 to Sep 2011] Worked at IBM Research Labs, Haifa on a project that aims to **adopt an existing processor core checking solution for accelerated simulation by intelligent collection of trace data**. This checking solution is targeted for pre-silicon validation of upcoming IBM POWER processor. This work has been published in DAC 2012 conference.
- [June 2011 to Dec 2011] Worked in collaboration with University of Verona researchers to boost the performance of **System-C simulation using parallel platforms such as GPUs**. This work has been published in DAC 2012 conference.
- [May 2011 – Sep 2011] Worked on novel solutions to **adapt complex pre-silicon checkers for simulation acceleration environments**. I worked on a concept of approximating checkers for simulation acceleration platforms so that checkers can be implemented with less logic resources and yet provide checking with acceptable rate of false positive or false negatives. The first phase of this work has been published in DATE 2012. This is a collaborative effort with IBM research.

- [Nov 2010 – April 2011] Worked on an **algorithm for trace signal selection for state restoration used in post-silicon debug**, which attempts to maximize number of restored states per observed trace signal. This work has been accepted for publication in ICCAD 2011 conference.

- [Aug 2009 – May 2010] Worked on a **high performance combinational equivalence checking tool called EQUIPE**, which utilizes massively parallel processing power of GPUs to achieve fast functional matching as well as formal techniques to solve equivalence checking for large industrial designs. This work was published in ICCD 2010 conference.

- [Mar 2008 to May 2009] Developed a **GP-GPU accelerated gate level logic simulator named GCS**, which is a number of times faster than commercial logic simulators. Further extended the cycle based simulator to an event-driven simulator. This work has been published in DATE 2009 and DAC 2009 conferences and has later appeared as a book chapter and as a journal paper.

- [Oct-Dec 2007] Designed **an out-of-order, fully 2 way superscalar processor** for a subset of DEC-alpha instruction set architecture in Verilog **resembling the Intel P6 architecture** as a part of advanced computer architecture course at University of Michigan. The processor had architectural features such as a branch predictor and out-of-order load store queue.

- [2006, 2007] Worked on a project (**sponsored by ISRO: Indian Space Research Organization**) on **Digital Land Cover Classification using Multi Sensor and Multi Source Data** with the guidance of Prof. Anjan Sarkar at IIT Kharagpur. The project involved generation of an alternate crop pattern from multi-source data, using mathematical techniques, fuzzy logic and neural networks. This resulted in an IJRS journal publication.

PROFESSIONAL EXPERIENCE

- [June 2013-present] **IBM STG Austin** – **Development Staff Member –** Developed and maintained simulation acceleration environment for validation of IBM POWER8 processor and derivative system level designs. Performed end-to-end validation of system-level designs with exercisers, which needed comprehension of the verification testcase, microarchitecture and sw/hw interface. Currently working on validation relating to Coherent Processor Attach Interface (CAPI) port of POWER8 and derivative designs.

- [Sept-Dec 2012] **University of Michigan** - **Graduate Student Instructor –** Taught discussion sections and carried out other instructor duties for a graduate level digital design verification course (EECS 578: Computer-Aided Design Verification of Digital Systems).

- [Jan-Apr 2012] **University of Michigan** - **Graduate Student Instructor –** Taught discussion sections and carried out other instructor duties for an undergraduate level computer architecture course (EECS 370: Introduction to Computer Architecture).

- [July-Sept 2011] **IBM Research, Haifa** – **Summer intern**- Project goal was to adapt a processor core checking solution for accelerated simulation by intelligent collection of trace data. This checking solution is targeted for pre-silicon validation of upcoming IBM POWER processor.

- [May-Aug 2010] **Advanced Micro Devices, Sunnyvale, Office of the CTO, GPU technology group** – **Summer intern**- Project goal was to develop a high level power model for the upcoming fusion line of processors (integrated CPU cores with a GPU on chip), which works at the granularity of driver API calls between the CPU and GPU and provides power estimate. The tool was used for design exploration.

- [Sept 2008-Apr 2013] **University of Michigan** - **Graduate Student Research Assistant -** Carrying out independent research in fields of electronic design automation, design validation etc. Have served as reviewer for major EDA and computer architecture conferences (DATE, DAC, ICCAD, ISCA, MICRO, HPCA) and journals (IEEE TC, TCAD, ACM TODAES).
- [May-July 2006] **Microsoft Research, Redmond, Network security group – Summer intern**- Project goal was to develop a software agent in C# to look for leaked private information such as telephone number, credit card numbers etc over the web and report such malicious sources.

ACHIEVEMENTS & AWARDS

- Was awarded the **NVIDIA Graduate Fellowship for the year 2010-2011**
- University of Michigan – EECS dept. – **Departmental Graduate Fellowship**
- Indian Institutes of Technology - Secured **317th position in IITJEE 2003** (out of more than172000 students all over India)

RELEVANT COURSES

- Computer Architecture (EECS 470)
- Parallel Computer Architecture (EECS 570)
- Enterprise Computer Architecture (EECS 598)
- Advanced Compilers (EECS 583)
- Computer-Aided Design Verification of Digital Systems (EECS 578)
- Management Presentations (LHC 561)

ADDITIONAL INFORMATION

- **Comprehensive Knowledge of C, C++**
- Compiler Tools Lex, Yacc
- **Hardware Description Language: expertise in Verilog, VHDL**
- Familiarity with testbench languages/frameworks: Fusion RTX, system-verilog and UVM
- HDL level and gate level simulation, testing, verification
- Assembly languages RISC: POWER, SPARC, Alpha, CISC: x86
- Scripting with shellscript, python, perl
- **Experience in GPGPU parallel programming frameworks NVIDIA CUDA, OpenCL**
- Experience in object-oriented programming using Java, C#
- Experience with tools like MATLAB, Microsoft visual studio
- **Languages known**:
    - English, Bengali, Hindi

PRESENTATIONS

- **"GCS: High-performance gate-level simulation with GPGPUs"** at DATE 2009, Nice, France, April 2009
- **"Event-driven gate-level simulation with GP-GPUs"** at DAC 2009, San Francisco, USA, July 2009.
- **"Activity-based Refinement for Abstraction-guided Simulation"** at HLDVT 2009, San Francisco, USA, November 2009
- **"EQUIPE: Parallel Equivalence Checking with GP-GPUs"** at ICCD 2010, Amsterdam, The Netherlands, October 2010
- **"High Performance Gate-level Simulation with GP-GPU Computing"** *invited talk at VLSI-DAT 2011*, Hsinchu, Taiwan, April 2011
- **"Simulation-based Signal Selection for State Restoration in Silicon Debug"** at ICCAD 2011, San Jose, USA, November 2011.

- **"Checking Architectural Outputs Instruction-By-Instruction on Acceleration Platforms"** at DAC 2012, San Francisco, USA, June 2012.

PROFESSIONAL REFERENCES

- Available on request